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... It would be incorrect if a later **load** issued prior to **...** not return the value of the earlier **store** to the **...** not know the memory **address** before the **instruction** issues **...**
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... gathered in previous executions of that static **load**/**store**. Predicted loads and **stores** are issued speculatively **...** **Instructions** that depend on **speculative** loads are **...**
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... If a **load** is to the same **address** as a **...** **store**, it can use data bypassed from the **store** when the **...** constraint of this approach is that a **load instruction** cannot be **...**
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... its **address** base is included in a p-slice, the **address** accessed by this **load** is also **...** When a **store instruction** (again with the stack register as its base) is **...**
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... are handled by augmenting the functionality of the **load-store** queues. ... and the program counter is set to the **address** specified by the last TRY **instruction**. ...
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... to dynamically control the out-of-order execution of **load-store instructions** in a processor ...
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... Floating Point **Instruction** PO • **Instruction** Fetch PO **Instruction** Fetch PI ... prior art by permitting **speculative** execution of **load** and **store instructions**. ...
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